#8/a
11/12/2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **OZAWA, Hiroyuki et al.**

Group Art Unit: **2815**

Serial No.: **09/994,753**

Examiner: **CLARK, SHEILA V.**

Filed: **November 28, 2001**

P.T.O. Confirmation No.: 8648

For: **SEMICONDUCTOR INTEGRATED CIRCUIT WITH DUMMY PATTERNS**

AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
Washington, D.C. 20231

November 5, 2002

Sir:

In response to the Office Action dated **July 5, 2002**, extended to **November 5, 2002** by a one-month Petition for Extension of Time, please amend the above-identified application as follows:

IN THE CLAIMS:

CANCEL claims 7, 9, 14, 15 and 16, without prejudice or disclaimer.

AMEND claims 4, 5, and 8 to read as follows:

4. (AMENDED) A semiconductor integrated circuit, comprising:

a plurality of layers provided on a semiconductor substrate;

wires provided in a first layer that is one of said plurality of layers; and

wire dummies provided in a second layer different from the first layer and having an arrangement that avoids areas overlapping positions of said wires,